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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/247,413	02/10/99	LO	Y NOVA-P033-T

022877
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IM52/0823

EXAMINER	
ANDERSON, M	
ART UNIT	PAPER NUMBER
1765	22

DATE MAILED: 08/23/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/247,413	LO ET AL.	
	Examiner	Art Unit	
	Matthew A. Anderson	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11,18,19 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-11,18,19,21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 2-4,7-8, 18-19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimbo et al. in view of Lee et al. (US 4,900,372) and Narayan et al. (US 5,208,182).

Shimbo et al. discloses the bonding of InP and GaP single crystal substrates in Figs. 2A and 2B. In Col. 1 lines 48-61, the known need for lattice constant match between the layer grown and the substrate during epitaxy is described. Lattice mismatch between layers is described as an important processing parameter. GaAs and AlGaAs are described as capable of forming a good heterojunction epitaxially. In Col. 3 lines 6-38 is described the process of Shimbo et al. The bonded substrates are annealed at between 200-600'C with the exact temperature depending on the substances being bonded. In lines 23-29 the thermal expansion mismatch of bonded substrates is described as preferably below 2×10^{-6}/=C. Otherwise, mechanical failure

(i.e. cracking) occurs at the boundary. The thermal expansion of bonded substrates is an important processing parameter. The bonded substrates described are GaAs/InP, ZnS/GaAs, InP/InSb, GaP/InP, CDs/InP, GaAs/ GaAs, InP/InP. In Example 4, a substrate of thickness 60□m was bonded to a second substrate.

Shimbo et al. does not describe the so formed device as a substrate for further fabrication.

Lee et al. discloses in the abstract a method of annealing deposited layers of III-V compound semiconductors when deposited on Si, Ge/Si, or other single crystal substrates. In Col. 3 lines 42+ is described the formation of thermal strain layers and buffer layer)s and their anneal cycle. Lee et al. in Col. 4 lines 1-17 describe typical buffer layers as GaAs, InGaAs, and AlGaAs. The second buffer layer is described as also annealed. One of ordinary skill in the art would recognize the anneal steps as for the purpose of reducing the crystal imperfections in the buffer layers. Described in col. 4 lines 5-21 is the need to optimize conditions depending on the material used.

Narayan et al. discloses the formation of a super lattice buffer layer and the repeating of the superlattice buffer layers until the buffer layer is greater than the critical thickness for bending the dislocations. In Col. 6 lines 3+, the method is described in more detail.

It would have been obvious to combine the references of Shimbo et al., Lee et al., and Narayan because Shimbo et al. produces a construct which would be useful as

a substrate and Lee et al. and Narayan disclose the formation of buffer layers on substrates of the same materials as the substrates of Shimbo et al. and because such a combination would have been anticipated to produce an expected result.

In regard to claim 21, it would have been obvious to one of ordinary skill in the art to form a bonded substrate from GaP, InP and to choose layers to be subsequently formed on that substrate to have compatible thermal expansion properties and lattice constant properties because the prior art recognizes that the these parameters need to be optimized according to the material used and these materials were known. The examiner notes that the bonded substrate of Shimbo et al is composed of the identical materials disclosed in the specification and therefore optimization of the these materials would have been anticipated to produce an expected result.

In regard to claim 2-4, it would have been obvious to one of ordinary skill in the art at the time of the present invention to grow a buffer layer on either face of the substrate because Lee discloses the formation of a buffer layer on a single crystal substrate (of which, a InP/GaP bonded substrate is one) and because such a combination would have been anticipated to produce an expected result.

In regard to claim 2, It would have been obvious to one of ordinary skill in the art at the time of the present invention to repeat the growing and annealing of the substrate because Narayan et al. discloses such buffer layer constructs that are added to until the

critical dislocation bending thickness is reached and such a process would have been anticipated to produce an expected result.

In regard to claims 18-19, it would have been obvious to one of ordinary skill in the art at the time of the present invention to optimize the thickness of the substrate layers because Narayan et al. discloses a critical thickness of dislocation bending which was known to yield reduced numbers of dislocations in subsequent epitaxially grown films(see col. 4-6 and especially col. 5 lines 40+ and col. 6 lines 1-2) and discloses a method of optimization of such thicknesses. Such optimization would have been achieved with only routine experimentation and would have been anticipated to produce expected results.

3. Claims 5-6, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimbo et al. and Lee et al. and Narayan et al. as applied to claim s 2-4,7-8, 18-19, 21 above, and further in view of Furuyama et al. (US 4,992,386).

Shimbo et al. discloses the bonding of InP and GaP substrates as described above.

Shimbo et al. does not describe further device fabrication.

Lee et al. discloses a method of annealing deposited layers of III-V compound semiconductors when single crystal substrates as described above..

Lee does not disclose further device fabrication after the buffer layer.

Narayan et al. discloses the formation of a buffer layer of critical thickness to bend dislocations as described above.

Furuyama et al. discloses a semiconductor device as is seen in Fig. 5. InP has GaInAs deposited thereon. InP is seen to be deposited thereon with a further deposition of InP (an InP based semiconductor).

It would have been obvious to one of the ordinary skill in the art at the time of the present invention to combine the references because all dealt with III-V semiconductors and the lattice engineering of the inherent thermal and lattice properties of the materials thereof and because such a combination would have been anticipated to produce an expected result.

In regard to claims 5-6, 11 it would have been obvious to grow a first epilayer (InP) on a buffer layer (GaInAs intermediate buffer layer) and a second epilayer (InP) on the first epilayer because such a growth sequence was suggested in the art (Furuyama et al.) and because such a growth sequence would have been anticipated to produce an expected result.

In regard to claims 9 and 10, it would have been obvious at the time of the present invention to one of ordinary skill in the art to form the buffer layer from AlGaAs, or InGaAs and the first and second epilayers from InP because such materials are suggested by the combined references and because such a use of these materials would have been anticipated to produce an expected result.

Conclusion

4. All claims are drawn to the same invention claimed in the parent application prior to the filing of this Continued Prosecution Application under 37 CFR 1.53(d) and could have been finally rejected on the grounds and art of record in the next Office action. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing under 37 CFR 1.53(d). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Anderson whose telephone number is (703) 308-0086. The examiner can normally be reached on Monday-Thursday from 6:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Benjamin Utech, can be reached at (703) 308-3836.

Any inquiry of a general nature can be directed to the group receptionist whose telephone number is (703) 308-0661.

MAA

August 22, 2001

FELISA HITESHEW
PRIMARY EXAMINER